IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

OKI AMERICA, INC. ET AL,

Plaintiff,

v.

ADVANCED MICRO DEVICES, INC.,

Defendant.
_____/

AND RELATED COUNTERCLAIMS
_____/

No. C 04-03171 CRB

MEMORANDUM AND ORDER

Now pending before the Court are motions by (1) plaintiff Oki America et al. (collectively "Oki") for partial summary judgment of (i) noninfringement of U.S. Patent No. 4,518,678 ("the Allen patent"); (ii) invalidity of U.S. Patent No. 4,737,830 ("the Patel patent"); (iii) invalidity of U.S. Patent No. 4,960,732 ("the Dixit patent"); (iv) infringement of U.S. Patent No.'s 5,739,571 and 5,856,694 ("the Kurachi patents"); and (v) infringement of U.S. Patent No. 6,495,855 ("the Sawamura patent"); and (2) defendant Advanced Micro Devices ("AMD") for partial summary judgment of (vi) literal infringement of the Patel patent; (vii) noninfringement of the Kurachi patents; and (viii) invalidity of the Sawamura patent.

Also pending before the Court are: (3) Oki's motion to strike the Mr. Ratliff reports under Daubert; (4) Oki's motion to strike the Dr. Smith report; (5) Oki's motion to strike portions of the Dr. Neikirk report; (6) AMD's motion to exclude portions of the testimony of

Mr. Troxel; (7) AMD's motion to exclude portions of the Dr. Fonash report; and (8) AMD's motion to exclude the testimony of Dr. Fair.

All of these evidentiary motions will be decided at the pre-trial conference. Only one motion, Oki's motion to strike the Smith report, relates to the merits of a pending motion for partial summary judgment, but a ruling on the Smith report is not dispositive of that motion. See infra.

I. BACKGROUND

This lawsuit involves the alleged infringement of patents related to devices and methods for use in the semiconductor industry. Six patents remain in the case. Oki is the assignee of three, and AMD is the assignee of three. All six patents are at issue in the pending summary judgment motions.

II. Legal Standard for Summary Judgment

Summary judgment is proper when "the pleadings, depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to a judgment as a matter of law." Fed. R. Civ. P. 56(c). An issue is "genuine" only if there is a sufficient evidentiary basis on which a reasonable fact finder could find for the non-moving party, and a dispute is "material" only if it could affect the outcome of the suit under governing law. See Anderson v. Liberty Lobby, Inc., 477 U.S. 242, 248-49 (1986). "Where the record taken as a whole could not lead a rational trier of fact to find for the non-moving party, there is no 'genuine issue for trial.'" Matsushita Elec. Indus. Co. v. Zenith Radio Corp., 475 U.S. 574, 587 (1986) (citation omitted).

A principal purpose of the summary judgment procedure "is to isolate and dispose of factually unsupported claims." See Celotex Corp. v. Catrett, 477 U.S. 317, 323-24 (1986). A party moving for summary judgment that does not have the ultimate burden of persuasion at trial has the initial burden of producing evidence negating an essential element of the non-moving party's claims or showing that the non-moving party does not have enough evidence of an essential element to carry its ultimate burden of persuasion at trial. See Nissan Fire &

Marine Ins. Co. v. Fritz Cos., 210 F.3d 1099, 1102 (9th Cir. 2000). Where the party moving for summary judgment would bear the burden of proof at trial, it has the initial burden of producing evidence which would entitle it to a directed verdict if the evidence went uncontroverted at trial. See C.A.R. Transp. Brokerage Co. v. Darden Rests., Inc., 213 F.3d 474, 480 (9th Cir. 2000).

If the moving party does not satisfy its initial burden, the non-moving party has no obligation to produce anything and summary judgment must be denied. If, on the other hand, the moving party has satisfied its initial burden of production, then the non-moving party may not rest upon mere allegations or denials of the adverse party's evidence, but instead must produce admissible evidence that shows there is a genuine issue of material fact for trial. See Nissan Fire & Marine Ins. Co., 210 F.3d at 1102.

Summary judgment is appropriate in a patent case, as in any other case, where there in no genuine issue of material fact and the movant is entitled to judgment as a matter of law. Nike Inc. v. Wolverine World Wide, Inc., 43 F.3d 644, 646 (Fed. Cir. 1994) (citations omitted). To invalidate a patent, a moving party must overcome the presumption of validity that inheres in a patent by clear and convincing evidence. 35 U.S.C. § 282; United States Gypsum Co. v. National Gypsum Co., 74 F.3d 1209, 1212 (Fed. Cir. 1996). Determination of infringement is normally a fact-intensive issue, but comparison of a properly interpreted claim with a stipulated or uncontested description of an accused process would reflect such an absence of material fact as to warrant summary judgment of infringement or noninfringement. Norian Corp. v. Stryker Corp., 433 F. Supp. 2d 1051, 1053 (N.D. Cal. 2004) (citing D.M.I. Inc. v. Deere & Co., 755 F.2d 1570, 1573 (Fed. Cir. 1985)).

For claim constructions addressed below, the Court incorporates the statements of law set forth in the Claim Construction Order, issued February 14, 2006.

III. Motion for Partial Summary Judgment of Noninfringement of the Allen Patent

1. Background

The Allen patent is entitled "Selective Removal of Coating Material on a Coated Substrate." '678 patent at [54]. AMD is the assignee. Id. at [73]. The patent is directed to

an improvement in the process for producing semiconductor devices comprising the selective removal of coatings from the periphery of a wafer to mitigate the inadvertent dislodgement of coatings from this area in subsequent processing steps. Id. at [57].

At many points in the semiconductor fabrication process there is a need to temporarily apply a thin coating to enable the treatment of selected regions on the surface of a wafer. The steps to accomplish this coating include spreading a thin liquid film over the wafer surface, followed by, for example, hardening the film, exposing the film to a light patterns, and selectively washing away either the exposed or the unexposed portions of the film. The liquid film is photosensitive, and generally referred to as a "photoresist." The photoresist is spread over the wafer by dropping the liquid onto the wafer center while spinning it. The centrifugal forces spread the liquid across the wafer towards the edge. The photoresist potentially accumulates, however, at the side edge and on the lower surface. These portions of the coating are subject to breaking off as fine particles during subsequent handling operations. Debris of this sort can interfere with device fabrication and lead to defects. See '678 patent at 1:13:63.

The Allen invention addresses these shortcomings by providing processes for removing the photoresist from the edge of the wafer in order to circumvent debris formation by resist at the periphery. See id. at 1:65 – 2:34, claims 1-12.

2. The Motion

AMD accuses Oki of infringing claim 5 of the Allen patent. Oki moves for summary judgment of noninfringement on the ground that the claim requires that photoresist be removed from the periphery of both sides of a wafer, and that because its coating process confines the photoresist to only one side, that is, there is no resist on the back side of the wafer, one of the elements needed to prove infringement cannot be met. AMD agrees, for the purpose of this motion, that the claim requires some resist to be removed from both sides of the wafer, but nonetheless asserts that factual evidence demonstrates that photoresist is present on the back side of the wafer in the Oki manufacturing process.

3. Analysis

Oki's Rule 30(b)(6) representative answered in response to a question about Oki's process that: "the objective is to dissolve the resist that has - the unnecessary resist that has adhered to the back surface and to dissolve the resist that is adhering to the edge." Curran Decl., Exh. H (Deposition of Mr. Katsuyama) at 60:24 - 61:2. Despite Oki's contention that the statement reflects the objective of the manufacturer of the wafer rinse equipment used by Oki, and not that of Oki, the context of the discussion surrounding the quoted passage supports an inference that in Oki's process the resist migrates to the wafer's back side.

The fact that a back side rinse is even performed also supports such an inference. Oki contends it uses the rinse equipment simply in the format as supplied by the manufacturer, that is, with rinse nozzles that address both the top side and back side of a wafer, and disabling the nozzle is unnecessary. But, even as Oki contends it gains no benefit from the back side nozzle, it nonetheless programs the backside nozzle for use and some equipment seems to only have had back rinse capabilities. See id. at 94:22 - 95:1.

Accordingly, a reasonable jury could resolve the issue of infringement in favor of the non-moving party, AMD. Vivid Tech., Inc. v. American Sci. & Eng'g, Inc., 200 F.3d 795, 806-07 (Fed. Cir. 1999) (the non-moving party need only establish that material facts relied on by the movant are not undisputed, or that the undisputed facts do not entitle judgment as a matter of law). The motion for summary judgment is therefore DENIED.

The Court need not address the motion to strike the Smith report at this time because the Smith report is not necessary to create a genuine dispute as to infringement.

IV. Cross-Motions for Partial Summary Judgment of Invalidity and Literal Infringement of the Patel Patent

1. Background

The Patel patent is entitled "Integrated Circuit Structure Having Compensating Means for Self-Inductance Effects." '830 patent at [54]. AMD is the assignee. Id. at [73]. The patent is directed to an improved integrated circuit design that includes "capacitance means"

wired between the busses and located in a layer beneath and along the length of one of those busses.

Faster, more powerful microprocessors require a more dense spacing of electronic elements, longer busses and more output pins. Operating the processors at increased clock speeds means faster switching times at the output pins. Together these factors lead to higher peak current transients, which induce voltage spikes due to self-inductance in the busses, wires and leads. The Patel patent acknowledges that those skilled in the art realized that such induced voltages adversely affect switching speeds within the chip and cause logic errors.

Rather than trying to design around the problem, the Patel patent discloses an improved circuit structure that would alleviate or compensate for induced voltage spikes. The claimed circuit includes one or more "MOS capacitors,"[1] coupled between the ground and power busses, fabricated directly beneath at least one of the busses. See id., Claim 1 at 6:15-41. Patel also discloses and claims that the capacitance means is/are to be "distributed along said busses" to thereby compensate for inductance effects in the busses. Id.

2. The Cross-Motions

AMD moves for literal infringement of claims 1, 2, 5 and 6. Oki's expert concedes infringement, but only if the claims are given the construction proposed by Oki. If the claims are construed as AMD proposes, however, Oki maintains that there is at least a genuine issue as to whether its practice infringes. The parties dispute the proper construction of the terms "electrode means," and "distributed along said busses" recited in claim 1, the only independent claim. Id. at 6:32, 39.

Oki cross-moves for invalidity of all six claims of the Patel patent based on their being either anticipated by, or obvious over U.S. Patent No. 4,654,689 to Fujii ("the Fujii patent"). According to Oki, the Fujii patent discloses the same MOS capacitors, that, moreover, serve the same purpose. The parties do not dispute the content of the Fujii disclosure; instead, their disagreement centers again on the same claim terms noted above, and whether they read on,

---

[1]The actual claim language reads "MGS capacitor;" the parties agree it is a typographical error.

or are obvious in view of, the Fujii invention.

3. Analysis

Claim construction of the disputed terms is a starting point common to both the infringement and anticipation analyses. Amazon.com Inc. v. Barnesandnoble.com Inc., 239 F.3d 1343, 1351 (Fed. Cir. 2001) ("Claims must be construed and given the same meaning for purposes of both invalidity and infringement analyses"); see also Markman v. Westview Instruments, Inc., 52 F.3d 967, 976 (Fed. Cir. 1995), aff'd, 517 U.S. 370 (1996) (analyzing patent infringement requires two steps: first, the asserted claims are construed, and second it is determined whether the accused method or product infringes the claims as properly construed); Lindemann Maschinenfabrik v. American Hoist & Derrick Co., 730 F.2d 1452, 1458 (Fed. Cir. 1984) (analyzing anticipation requires identifying the elements of the claims, determining their meaning in light of the specification and prosecution history, and identifying corresponding elements disclosed in the allegedly anticipating reference). The Court finds unpersuasive AMD's attempt to construe the disputed claim terms to avoid anticipation over the Fujii patent, but claims 5 and 6 of Patel are not obvious over the same.

a. Construction of "electrode means"

The first term in dispute concerns the "electrode means" for connecting one of the capacitor plates to the circuit. The full claim limitation reads: "electrode means comprising a source/drain in said substrate contiguous with said doped region and electrically connecting said doped region of said MOS capacitor to the other of said busses." '830 at 6:32-35. Despite use of the term of art "means," this limitation is not a means-plus-function limitation subject to interpretation under 35 U.S.C. section 112, ¶ 6 because the language thereafter provides a sufficient substantive description of the electrode structure. Micro Chem. Inc. v. Great Plains Chem. Co., 194 F.3d 1250, 1257 (Fed. Cir. 1999) (the presumption that section 112, ¶ 6 applies "collapses, however, if the claim itself recites sufficient structure, material, or acts to perform the claimed function").

The plain meaning of "source/drain" is not fully apparent from the claim itself, but its location and function is readily understood from the whole of the claim. The "source/drain"

is understood to be embedded in the substrate. The "doped region," whose antecedent basis is found in element (b) of claim 1, likewise is embedded in the substrate, being formed in the substrate at a location beneath a gate electrode. The limitation that the source/drain is contiguous with the doped region introduces the notion that not only are they both within the substrate, but the two regions meet at an interface. Furthermore, this interface provides electrical communication between the two regions because the claim also requires that the doped region be electrically connected to one of the busses via the source/drain.

Claim 1 marks the only recitation of "source/drain" in the entire patent, but the phrase is readily understood to refer to, in the aggregate, the source and drain "regions" described in the specification. The terminology of source and drain is borrowed from transistor technology, and the analogy is further strengthened by the choice of a capacitor in the form of a "MOS capacitor" to illustrate the invention. The figures used to illustrate an embodiment of the invention show what would be the source, drain, channel, insulating oxide layer and gate of an MOS transistor, but used in the invention to function as a capacitor.

The analogy between the capacitor of the invention and a transistor, however, has its limits. In another embodiment, an additional region is embedded in the substrate that interconnects the source and drain regions–a feature that would render a transistor nonfunctional. This embodiment is said to offer the additional advantages of lowered resistance in the pathway between the lower capacitor plate and the bus, as well as alternate locations at which to form the connection to the bus. Thus, one skilled in the art would understand that the terms source and drain do not impart the limitations appurtenant to transistors, but instead loosely indicate the method of formation (doping), and the general location (within the substrate contacting a channel--here called the "doped region"), of these regions. The term "source/drain," coined specifically in claim 1, reflects the teaching of the specification that the otherwise distinct regions may be connected and function as one aggregate.

Based on the foregoing, the Court construes the phrase "electrode means comprising a

source/drain" to mean a region or regions embedded in a semiconductor substrate that forms an interface with the lower capacitor plate, which is the doped region embedded in the substrate that lies beneath the gate electrode, and the region or regions electrically connect the lower plate to one of the busses.

b. Construction of "distributed along said busses"

The second disputed phrase, "distributed along said busses," acquires different meanings depending on whether there is "one," or there are "more [than one]" MOS capacitors comprising the capacitance means. See '830 patent at 6:21. The ordinary meaning of "distributed" is dispersed, spread, or meted out. Where the word is used to describe a single substance or article, it connotes that the substance or article is spread out. In the context of the claims, the capacitance means, that is, the capacitor plates, would be spread out along (and underneath) the busses. In the alternate case of a plurality of capacitance means, the plain meaning is that the capacitors are located at various positions along (and underneath) the busses. Also implicit in this terminology is the suggestion that the longer of the lateral dimensions of the capacitor plates is along the direction of the bus wires, and the transverse dimension is shorter. This suggestion is strongest when there is only one capacitor, but as the number of different capacitors distributed along the device increases, the weight of the meaning imparted to "distributed along" shifts to the connotation that the individual parts are dispersed, not just anywhere over the chip, but along the busses.

The specification does not discuss in any detail what is meant by "distributed along said busses" so as to substantively limit the plain meaning of the claim. There is no teaching with respect to the meaning of distributed when there is only one capacitor. For example, the disclosure does not imply, as AMD contends, that a single capacitor must run underneath the entire length, or a substantial part of the busses. The specification does allow for "empirical observations" to guide the practitioner in determining how much capacitance might be needed in a particular circumstance. '830 patent at 5:10. The disclosure simply does not teach what minimum level of distribution of capacitance means is required by the claims.

The Court construes the term "distributed along said busses" to mean either multiple capacitance means located at various points along, and in a layer beneath, the busses, or a single capacitance means having plates whose long dimension is spread out along, and in a layer beneath, the busses. The Court does not read in any minimum fraction of the length a bus along which capacitance means must be deployed. The disclosure instructs that empirical observation may be the guide.

c. Anticipation by the Fujii patent

Having construed the elements of the claims, the next step is to identify corresponding elements disclosed in the Fujii patent, the allegedly anticipating reference. Lindemann, 730 F.2d at 1458. The Fujii patent teaches a "MOS type capacitor" constructed beneath the power supply wiring layers that operates to "decrease the surge current induced in the wiring layers by the capacitor." See Fujii patent at [57]. The disclosure teaches that the capacitor is constructed of upper and lower electrodes: the upper being a "silicon plate," and the lower being a doped impurity region embedded in the substrate. Id. at 4:60-62, 5:1-3. The Fujii patent also discloses that in one embodiment of the invention, a single MOS capacitor lies underneath and along the bus wires for a majority of the length of the processor chip. See id. at Fig. 5.

The corresponding elements of the "doped region" and "source/drain" of Patel are found in Fujii. Patel does not require the doped region and the source/drain region to be either distinctly doped, that is, of different polarity, or to have a different degree or level of doping. As noted above, the analogy between the capacitor and a transistor has its limits, and one of skill in the art would not presume that requirements for functionality in a transistor would likewise apply to the capacitance means of the invention. Fujii, who also refers to the structures as "MOS capacitors," expressly discloses the instance in which the two regions are similarly doped.

The two regions of Patel are distinct insofar as the doped region lies entirely beneath the upper electrode, which in both cases is a silicon gate [plate], and the source/drain region extends laterally beyond the perimeter of the capacitor plates and permits a vertical

connection to another layer within the device. These "distinct" elements exist in Fujii, and therefore Fujii anticipates this claim limitation. See, e.g., In re Kelley, 305 F.2d 909, 914 (C.C.P.A. 1962) ("[w]e see no reason why a single structural element . . . which performs two separate functions, cannot support a claim reciting broadly these separate functions"). Finding two structural elements (the lower plate and the electrode means) in the uniformly doped region of Fujii does not require "arbitrary divisions of a single element" because they each occupy a distinct space and perform distinct functions. See In re Kelley, 305 F.2d at 915 (collecting cases distinguishing and following Kreidel v. Parker, 97 F.2d 171, 173 (C.C.P.A. 1938)).

An issued patent warrants a presumption of novelty. In examining the Patel patent, the examiner did not consider the Fujii patent as a prior art reference. Regardless of whether the reference was considered, however, the issued patent can only be invalidated by clear and convincing evidence. See American Hoist & Derrick Co. v. Sowa & Sons, Inc., 725 F.2d 1350, 1359-60 (Fed. Cir. 1984) (discussing the production of prior art not considered by the PTO: "neither does the standard of proof change; it must be by clear and convincing evidence"). The disclosure by Fujii of MOS-type capacitance means located along and beneath the bus wires of a semiconductor chip is a clear and enabling disclosure of all the limitations found in claims 1, 3, and 4 of the Patel patent. Claims 1, 3, and 4 of Patel are invalid under section 102(e) over the Fujii patent.

d. Obviousness in view of the Fujii patent

Oki also contends that claims 2, 5, and 6 are obvious over Fujii, and thus invalid under 35 U.S.C. section 103, because these claims "simply require the use of more than one of the MOS capacitors [of] claim 1." Mot. at 14. A determination of obviousness requires a suggestion or motivation to modify the reference to the claimed invention. Sibia Neurosciences Inc. v. Cadus Pharm., Inc., 225 F.3d 1349, 1356 (Fed. Cir. 2000); see also Graham v. John Deere Co., 383 U.S. 1, 17-18 (1966) (obviousness is a question of law, to be reached in light of an assessment of facts responsive to the Graham inquiries). The suggestion or motivation may derive from, among other sources, the knowledge of one of

skill in the art, or the nature of the problem to be solved. See Motorola, 121 F.3d at 1472.

The inventions of Fujii and Patel solve the problem of suppression of voltage spikes in the power supply lines. Where one capacitor is found to be insufficient, or other areas of the chip need to likewise be addressed, the use of additional capacitors would be obvious. Claim 2 simply recites a plurality of the MOS capacitors of claim 1. The use of multiple capacitors in parallel, as claim 2 would require, would have been recognized as a standard circuit design to those skilled in the art. Motorola, 121 F.3d at 1472 ("[T]he motivation to combine may come from the prior art, as filtered through the knowledge of one skilled in the art.").

The additional limitations of claims 5 and 6 are not obvious over Fujii.[2] First, these claims do not simply require, as Oki primarily contends, a plurality of MOS capacitors as recited in claim 1; instead, the claims introduce a limitation wherein for each doped region (lower plate), the gate electrode (upper plate) is divided into a plurality of segments, and each is separately wired to the bus. '830 patent at 6:53-58. A plurality of parallel capacitors is claimed, but it is not formed by replicating the structure of claim 1. The scope of Fujii does not include any type of variation on the structure of capacitors, nor does it suggest that defects in the insulating oxide film is an issue that could benefit from alternate designs. Oki has not shown that any suggestion or motivation to modify Fujii, if even present, rises to the level of clear and convincing evidence that is needed to support a determination of obviousness. See Kahn v. General Motors Corp., 135 F.3d 1472, 1480 (Fed. Cir. 1998).

e. Infringement of the Patel patent

Because claims 1-4 are invalid, there can be no infringement liability.[3] Medtronic,

---

[2]The action taken by the European Patent Office rejecting Patel's counterpart application over the same Fujii reference is neither controlling nor persuasive. Heidelberger Druckmaschinen AG v. Hantscho Commercial Products, Inc., 21 F.3d 1068, 1072 n.2 (Fed. Cir. 1994) ("Caution is required when applying the action of a foreign patent examiner to deciding whether the requirements of 35 U.S.C. § 103 are met under United States law, for international uniformity in theory and practice has not been achieved."). Courts in the United States do not defer to decisions in foreign courts or patent offices on questions of validity. See, e.g., Lindemann, 730 F.2d at 1458, n.2 (conceding that a reference was anticipatory to a foreign patent office deemed "meaningless" with respect to the issue of validity in the United States where the laws are different on that point).

[3]AMD moved for summary judgment of infringement only for claims 1, 2, 5, and 6.

Inc. v. Cardiac Pacemakers, Inc., 721 F.2d 1563, 1583 (Fed. Cir. 1983). Claims 5 and 6 are, however, subject to a finding of infringement liability. Oki concedes that if its preferred construction of the claims is adopted, then the accused products infringe the claims of the Patel patent. Oki Opp. Mot. (Document 477) at vi, 7, 12. Oki's expert witness made this concession at deposition because he also contended that given such a construction, the claims would be invalid in view of Fujii. For the reasons described above, the Court finds that even though four claims are invalidated by Fujii, the teachings of that reference do not render the last two obvious. Based on party admissions and the proffered evidence, the Court concludes that summary judgment of literal infringement of claims 5 and 6 by Oki's accused DRAM products is required.

Oki's motion for partial summary judgment of invalidity of the Patel patent is therefore GRANTED as to claims 1, 3, and 4 for anticipation by the Fujii patent, and as to claim 2 for obviousness in view of the same, and DENIED as to claims 5 and 6.

AMD's motion for partial summary judgment of infringement is DENIED as moot for claims 1 and 2, and GRANTED for claims 5 and 6.

V. Motion for Partial Summary Judgment of Invalidity of the Dixit Patent

1. Background

The Dixit patent is entitled "Contact Plug and Interconnect Employing a Barrier Lining and a Backfilled Conductor Material." '732 patent at [54]. AMD is the assignee. Id. at [73]. The patent is directed to a process for forming stable, low resistance "contact plugs" in "contact holes" as part of the fabrication of integrated semiconductor devices. The contact plugs serve to electrically join metal interconnects patterned on top of the protective overlayers with particular doped regions at the underlying semiconductor surface.

The Dixit invention addresses the issue of how to fill the contact hole with conductive material, called a "contact plug," as the hole size becomes smaller in diameter. Standard sputtering techniques that are used for wider holes fail to deposit adequate amounts of

material[4] at the bottom of the narrower holes. The Dixit patent discloses a process in which a contact hole is etched through the dielectric layer, the hole is lined with an adhesion and contacting layer, which is then coated with a barrier layer before finally substantially filling the contact hole with a conductive material. Several methods for filling the hole to form the contact plug are disclosed in the specification.

2. The Motion

Oki moves that the asserted claims of the Dixit patent are invalid under 35 U.S.C. section 102 or 103 for either being, respectively, anticipated by, or obvious over U.S. Patent No. 4,640,004 issued to Thomas ("the Thomas patent").[5] Oki contends that the only dispute between the parties as to whether Thomas anticipates the Dixit patent is over the construction of the term "contact plug." Oki asserts further that the Court's earlier construction of the limitation containing that term does not limit the plug to any particular size or shape, and that given such a broad reading, the claims of Dixit are anticipated by the disclosure of Thomas. AMD responds that Oki has failed to meet its burden of proof: first, the term contact plug was not directly addressed before; properly construed to cover only certain sizes and shapes, "contact plug" is not found in the Thomas patent, and second, the corresponding contact holes of Dixit are also not disclosed by Thomas.

3. Analysis

a. Construction of "contact plug" and "contact holes"

The parties did not previously ask the Court to construe "contact plug" or "contact holes," thus consideration of the size and shape of these features was not before the Court until now. In the Markman proceeding, the parties sought a construction of the process limitation "forming a contact plug comprising a conductive material which substantially fills said contact holes and which is in contact with said barrier layer." '732 patent at 7:54-56. The Claim Construction Order construes this limitation as "[t]he hole is plugged and thereby

---

[4]Coverage at the bottom of the hole is referred to as the "step coverage." '732 patent at 1:26-30.

[5]AMD is asserting claims 1, 4-7, 9, 10 and 13 against Oki.

substantially filled with a conductive material. This plug is in contact with the barrier layer." Order, Feb. 14, 2006, at 23:11-12. Nothing regarding the size or shape can be read into the prior construction because the purpose was to clarify whether the patentee disclaimed a plug that forms one continuous structure with a metal interconnect. See id. at 20:10-14.

To resolve the invalidity motion, the Court now construes the terms "contact plug" and "contact holes." See Lindemann, 730 F.2d at 1458. Both terms must be considered because each term acts to define the other.

The parties agree that "contact holes" are vertical-walled openings through an oxide layer that expose an underlying semiconductor region. The plain meaning of the claim language "contact holes of substantially uniform size" can be read in two ways: either to mean an opening of unvarying cross-section, that is to say, the walls are substantially vertical, or, that the plurality of openings are of the same size at, for example, the top surface. These connotations are not mutually exclusive; both may be read into the claim. The specification makes clear, however, and the parties do not dispute, that with respect to the profile of a hole, the claim is limited to vertical-walled holes. See, e.g., '732 patent at 4:15-19.

The parties do not agree whether the contact holes, and therefore the plugs that fill those holes, must have some particular width, height, or ratio of the two. AMD's contention that the hole must have a certain aspect ratio attempts to prove too much; the intrinsic evidence does not expressly support any such limitation. On the other hand, Oki's argument that the holes are not limited to any particular size overreaches. Although the claims are silent with respect to the dimensions of the holes and plugs, the specification and prosecution history provide the necessary basis to understand the claim scope even if it cannot be stated with numerical precision.

Plugs, the parties agree, are contacts (i) formed of a conductive material that (ii) substantially fill a "contact hole,"(iii) the hole having vertical walls. The dispute turns on what more is necessary to render something a plug. Implicit in the briefing on this issue is that the fact that the walls are vertical marks a difference between a plug and a non-plug.

Oki's expert witness testified as much: "[t]he basic definition of a plug as I – as I understood it – understand it and had used it back at this time was a vertical wall structure." AMD's Opp., Exh. O (Fonash Deposition) at 41-42; see also Markman, 52 F.3d at 986 (in construing disputed terms in claim language . . . [,] the focus in on . . . what one of ordinary skill in the art at the time of the invention would have understood the term to mean). The patentee also made the same distinction in prosecuting the patent, describing sloped wall contacts as "non-plug" contacts and vertical wall contacts as plug contacts. AMD's Opp., Exh G (Office Action Response) at 9, 11.

A vertical-walled hole of any diameter or size is not, however, filled by a plug. The Dixit patent explicitly teaches, and the parent patent[6] claims, plugs are contacts that fill holes up to 1.4 m in diameter (2 m^2 area), setting at least a lower size range for a plug according to the patent. The examiner ultimately agreed that Thomas, which disclosed openings of approximately 5.6 m in diameter (25 m^2 area), does not disclose a "plug," but Thomas also only discloses non-sloped walls; therefore, Thomas does not firmly establish an upper size range that would be considered to be a non-plug contact. It is possible that the hole size used as an example in Thomas is wide enough that the contact would not be considered to be a "plug" by those in art, that is, the slope of the wall may not be dispositive; however, that does not need to be decided here. That there is a distinction at all between plug and non-plug means that at some size it does matter whether the walls are sloped. The Dixit patent specification implicitly disclaims holes that can be filled by sputtering techniques without a step coverage problem. See, e.g., '732 patent at 1:26-30. Only holes that are large enough in size, or have sufficiently sloped walls, can be effectively filled using sputtering without suffering from a step coverage problem. Conversely, the invention claims a process that overcomes poor step coverage by forming "plugs" in "contact holes." Thus, the scope of the term "contact plug," as used in the patent, is a contact formed in a hole small enough in size that conventional sputtering techniques would otherwise fail to form a plug because of a step coverage problem.

[6]U.S. Patent No. 4,884,123

The deposition testimony of one of the inventors supports this description of the claim scope. When asked what he meant by the contact hole having a high aspect ratio, the inventor replied: "I would give a subjective answer, and the answer – and the subjective answer is one that cannot be filled directly by metal sput – by aluminum sputtering." Oki's Reply Br., Curran Decl., Exh. D (Klein Deposition) at 40:16-19. Distinguishing the invention through terms such as plug and non-plug is adequate because inventions do not have to be claimed in numerically precise terms. Modine Mfg. v. U.S. Int'l Trade Comm'n, 75 F.3d 1545, 1557 (Fed. Cir. 1996) (a patentee has the right to claim the invention in terms that would be understood by persons of skill in the art).

b. Application of the constructed terms to the motion

Thomas does not disclose the contact plugs that fill the contact holes of Dixit, either because Thomas does not disclose vertical-walled contact holes, or the holes described in Thomas are too wide to render the contact a plug. See Constant v. Advanced Micro Devices, Inc., 848 F.2d 1560, 1570 (Fed. Cir. 1988) (to anticipate a patent claim, a prior art reference must disclose, either expressly or inherently, each and every limitation of the claim). The openings in Thomas are taught to be the result of forming "islands of silicon dioxide" by growth or deposition, processes that can only produce sloped sidewalls. '004 patent at 3:14-17. This point alone is dispositive of the question of anticipation. The point at which a vertical-walled hole is of a small enough diameter to render the contact a plug, that is, what aspect ratio defines a plug, is a line that the court neither needs, nor seeks, to draw.

Oki's contention that the figures of Thomas illustrate vertical sidewalls, and therefore anticipate the Dixit invention, is unavailing because the specification is completely silent on this issue of the hole profile. See Nystrom v. Trex Co., Inc., 424 F.3d 1136, 1149 (Fed. Cir. 2005) ("unstated assumptions in prior art patent drawings cannot be the basis for challenging the validity of claims reciting specific dimensions not disclosed directly in such prior art"); Hockerson-Halberstadt, Inc. v. Avia Group Int'l, Inc., 222 F.3d 951, 956 (Fed. Cir. 2000) ("[i]t is well-established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely

silent on the issue).

Although Oki moves for summary judgment of invalidity under sections 102 and 103, it advances no argument for an obviousness determination other than that an anticipating disclosure also renders the claims obvious. Oki's motion for partial summary judgment of invalidity is therefore DENIED.

VI. Cross-Motions for Partial Summary Judgment of Infringement and Noninfringement of the Kurachi Patents

1. Background

The two Kurachi patents are both entitled "Semiconductor Device Having Protection Device for Preventing the Electrostatic Breakdown of Output Buffer MOSFETs." '571 patent at [54]; '694 patent at [54]. The '694 patent is a continuation of the '571 patent. The specifications of the two patents are the same. These patents are directed to semiconductor devices having integrated circuits in which the output buffer circuitry[7] is protected from electrostatic discharges by a protection circuit.

The invention addresses the following shortcoming. The output buffer circuitry is comprised of buffer MOSFETs,[8] which are ordinarily subject to electrostatic breakdown in the event of an electrostatic discharge on the device. A discharge changes the electrical potential in the semiconductor device. Should the potential exceed a certain level in the vicinity of a MOSFET (such as the buffer MOSFETs), control over the potential of the transistor gate is lost and thus control over the circuit is lost. The discharge can also permanently damage the device.

The inventions disclosed in the Kurachi patents seek to prevent the problems caused by electrostatic discharges by including a protection circuit, comprised of protection

---

[7]The output buffer circuitry is the means by which signals are output from the semiconductor device (more colloquially, the "chip") to the rest of the electronic circuit. Because this is the point of connection between the chip and other off-board, macroscale components that are more exposed to the environment, this portion of the chip is the most susceptible to such discharges.

[8]MOSFET stands for "metal oxide semiconductor field-effect transistor." A transistor is an electrical component in which the flow of current in a circuit can be reversibly switched between an "on" state and an "off" state by controlling the potential of a "gate."

MOSFETs, that is constructed and wired into the circuit in a particular manner so as to prevent a discharge from interfering with or damaging the buffer MOSFETs. As originally filed, the application also had claimed "protection pn diodes," but these claims were cancelled during prosecution following a rejection under section 103.[9] The disclosure by Kurachi of pn diodes remains in the written description and the figures of the issued patent. See, e.g., '571 patent at 10:65 - 11:63, Fig.'s 9, 10.

The Claim Construction Order issued by this Court construed the term "protection MOSFET," which appears in each of the asserted claims. The construction concludes that a MOSFET "has a source region, drain region, channel region, and a gate located above a thin insulating layer," and that a protection MOSFET is "a MOSFET connected to a circuit in such a way that it tends to prevent one or more circuits from undergoing electrostatic breakdown." Order, Feb. 14, 2006, at 10:15-18. The Court also emphasized that the protection MOSFET limitation draws its meaning primarily from its structure rather than its function. Id. at 7-10.

2. The Cross-Motions

Oki moves for partial summary judgment of infringement either literally, or under the doctrine of equivalents, of claims 1-3 of the '571 patent and claims 1, 3, and 4 of the '694 patent by AMD's K7 microprocessors, which were manufactured at the Fab 25 facility in Austin, Texas. AMD responds that because Oki has conceded it cannot seek damages but only injunctive relief, and because AMD stopped producing the K7 line before this action began, there is no case or controversy that supports jurisdiction. AMD also contends that at least one claim limitation is not present in its products.

AMD cross-moves for noninfringement by its K8 microprocessors, and for denial of injunctive relief as to the discontinued K7 product line. With respect to the K8 products, AMD asserts that it does not use "protection MOSFETs" as required by the claims; instead, K8 microprocessors use a "lubistor," a structure based on pn diodes. Oki responds that the

[9]The independent claim containing the pn diode limitation read, in relevant part: "said protection circuit having protective pn diodes for preventing electrostatic breakdown of the buffer MOSFETs."

lubistor infringes under the doctrine of equivalents, or that there is at least a factual dispute as to whether the claims cover AMD's lubistor under the doctrine of equivalents. Oki also contends that the past infringement by the K7 products constitutes an injury-in-fact that is subject to redress through the issuance of a declaration of infringement.

3. Analysis

a. Motions regarding the K7 microprocessors

Oki has agreed not to seek damages for any period prior to the time actual notice of infringement was given to AMD. Oki's Mot. at 3; AMD's Opp., Ryan Decl., Exh. F at 2 (memorializing Oki's stipulation). The parties agree that the accused K7 microprocessors were not made or sold by AMD after AMD had received actual notice of infringement.[10] Furthermore, Oki waived its right to establish marking of its own products that practice the Kurachi patents; as a consequence damages are unavailable by statute. 35 U.S.C. section 287(a); see also Lans v. Digital Equip. Corp., 252 F.3d 1320, 1326-27 (Fed. Cir. 2001).

With damages unavailable, Oki moves for a declaration of infringement and an injunction barring future manufacture and sale of products having the ESD protection circuitry as was present in the K7 microprocessor product lines. The Court concludes that, absent a controversy, it is without power to grant either.

Oki accuses several products of infringing the Kurachi patents, but jurisdiction must be considered separately as to each. See Sierra Applied Sciences, Inc. v. Advanced Energy Indus., Inc., 363 F.3d 1361, 1373 (Fed. Cir. 2004) (deciding jurisdiction separately for three distinct power supplies). A declaration of infringement by a patent holder against an alleged infringer represents a less common alignment of parties, but nonetheless is permitted under the law. Lang v. Pacific Marine and Supply Co., 895 F.2d 761, 763 (Fed. Cir. 1990). However, jurisdiction under Article III of the United States Constitution must be established, which requires there to be a "real and substantial controversy admitting of specific relief

[10]The parties do disagree as to whether notice occurred upon a request by Oki for leave to file its Second Amended Complaint (Feb. 10, 2005), or upon filing by Oki of its Final Infringement Contentions (May 1, 2006), but the dispute is moot because AMD's cessation predates both.

through a decree of a conclusive character, as distinguished from an opinion advising what the law would be upon a hypothetical state of facts." Aetna Life Ins. Co. of Hartford, Conn. v. Haworth, 300 U.S. 227, 241 (1937).

With respect to suits in which the patent holder is seeking a declaratory judgment, two elements must be established: (1) the defendant is engaged in an activity directed toward making, selling, or using subject to an infringement charge under 35 U.S.C. § 271(a), or be making meaningful preparation for such activity; and (2) acts of the defendant indicate a refusal to change the course of its actions in the face of acts by the patentee sufficient to create a reasonable apprehension that a suit will be forthcoming. Pacific Marine, 895 F.2d at 764.

Neither of these conditions is met in the present case. First, as the parties agree, AMD is no longer engaged the manufacture of the accused K7 products. Second, rather than AMD showing defiance, it had already changed its course and stopped producing microprocessors containing the allegedly infringing designs prior to the initiation of this suit. Furthermore, AMD has transitioned to a different processor core; moving back to a design that includes the old, allegedly infringing components would entail a huge expenditure of time and resources, and there are no allegations to this effect. AMD's conduct does not support a finding that a controversy that is sufficiently real and substantial exists. See id. at 764-65.

Oki contends that an injunction does not become moot simply because the conduct has stopped because AMD would be free to resume their prior activities; instead, an injunction is proper unless AMD meets the heavy burden of providing persuasive evidence that further infringement will not take place. See, e.g., Adarand Constructors, Inc. v. Slater, 528 U.S. 216, 222 (2000); Anderson v. Evans, 371 F.3d 475, 479 (9th Cir. 2004); W.L. Gore & Assoc., Inc. v. Garlock, Inc., 842 F.2d 1275, 1281-82 (Fed. Cir. 1988). In W.L. Gore, the injunction was affirmed because, although the accused infringer had stopped making the product at the time of the trial, there was no evidence that it no longer had the capacity to produce, or that the equipment had been sold or dismantled, or that it had no intention to resume production. Here, in contrast, the accused activity ceased prior to the suit, AMD's

current microprocessor products employ a different design, the Fab 25 facility used to make the K7 products has been sold off, and AMD has affirmed in public its intention to no longer make such designs.

The waiver of damages for past infringement, and the lack of a sufficiently concrete dispute regarding future infringement, together deprive the Court of jurisdiction. When the relief sought, a declaration of infringement and an injunction, would no longer make a difference to the legal interests of the parties, a case becomes moot. DeFunis v. Odegaard, 416 U.S. 312, 319-20 (1974). Oki's motion for partial summary judgment of a declaration of infringement of the Kurachi patents by the K7 products and the request for injunctive relief is therefore DENIED for lack of jurisdiction, and AMD's motion to deny injunctive relief to Oki with respect to the K7 product line is GRANTED.

b. Motion regarding the K8 microprocessors

AMD moves for a judgment of noninfringement of the Kurachi patents by its K8 products. Oki concedes that the products do not literally infringe, but that infringement should be found under the doctrine of equivalents, based on the argument that AMD's "lubistors,"[11] having a more complicated, three-layer structure than the disclosed two-layer pn diodes, are a later arising technology that is equivalent to the claimed protection MOSFETs. See Oki's Opp. at 7-8.

AMD contends that Oki is barred under prosecution history estoppel, namely the Festo presumption, from asserting the doctrine of equivalents. See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., 535 U.S. 722, 739-40 (2002). Specifically, AMD contends that Oki cancelled original claims 4 and 6 of the '571 patent, which recited a protection circuit having "protective pn diodes for preventing electrostatic breakdown of the buffer MOSFETs," to overcome a prior art-based rejection by the PTO, and therefore must be estopped from reaching any protection circuit based on pn diodes under the doctrine of

[11] Lubistor stands for lateral, unidirectional, bipolar-type insulated-gate transistor. Such a device has three main features: (i) a lateral p+/n/n+ or p+/p/n+ structure; (ii) an insulated gate above the middle doped region (either n or p); and (iii) the thickness of the middle region is equal to, or less than the effective Debye length

equivalents. See id. at 740; see also Schriber-Schroth Co. v. Cleveland Trust Co., 311 U.S. 211, 220-21 (1940) (cancellation of a claim in response to a prior-art rejection can create an estoppel as to the subject matter relinquished by the cancellation).

In Festo, the Supreme Court adopted a rebuttable presumption that an applicant who narrows a claim by amendment in order to avoid the prior art or to comply with 35 U.S.C. section 112 disavows his claim to the broader subject matter. Festo, 535 U.S. at 737. The patentee bears the burden of rebutting the presumption by showing that (i) the equivalent was unforeseeable at the time of the application, (ii) the rationale behind the amendment bears no more than a tangential relation to the equivalent, or (iii) some other reason why the patentee could not reasonably be expected to describe the "insubstantial substitute in question." Id. at 740-41. Oki has only raised the first ground as a basis for rebutting the presumption; that is, the "lubistor" was an unforeseeable equivalent at the time of the amendment cancelling the claims, and thus should not be precluded by prosecution history estoppel. The scope of how much of the territory between the original claims and the issued claims was ceded by prosecution history estoppel is a question of law for the Court to determine. See Warner-Jenkinson Co. v. Hilton Davis Chem. Co., 520 U.S. 17, 39, n.8 (1997); Glaxo Wellcome, Inc. v. Impax Labs., Inc., 356 F.3d 1348, 1352 (Fed. Cir. 2004).

AMD has offered evidence that lateral diodes and certain types of lubistors were known in the art prior to the time Oki cancelled the pn diode subject matter by amendment. For example, lateral pn diodes fabricated on top of an insulating oxide were first reported in 1982, and the use of such lateral pn diodes for protection of MOSFET output buffers from electrostatic discharge was disclosed in a patent filed in 1992 in Japan. AMD's Mot., Ryan Decl., Exh. N (Japanese Kokai Patent App. No. Hei 4-241452). Oki counters that these devices employed a different structure to insulate the lubistor from the MOSFETs, and it was not until a time nearly coincident with the amendment that lubistor protection circuits with the same type of shallow trench isolation used in the K8 microprocessors was published. This argument is unavailing because the type of isolation structures used in the prior art is not relevant to whether lubistors were known by those skilled in the art.

AMD has established as a matter of law that lateral pn diodes were known in the art at a time prior to the amendment in December, 1996, and that despite the more complicated structure, those skilled in the art recognized a "lubistor" to be a diode, albeit a diode having different fabrication requirements. Although the written description of the Kurachi patents only disclosed a "vertical" two-layer pn diode, the original claims used broader language that would have encompassed more than that which was revealed by the figures and written description. Those claims were cancelled without prejudice, but Oki also did not pursue those claims again in any subsequent application. Moreover, the examiner's rejection of the claims was not based on the particular structure disclosed by Oki, but rather on the diode as a circuit element, broadly defined. The rejected claim was simply drawn to "protective pn diodes," therefore the estoppel created cannot be said to be founded on the structure. Because lateral diodes were known in the art, and Oki had once submitted claims broadly covering pn diodes as a protection circuit element but abandoned those claims, Oki may not now recover, by the doctrine of equivalents, semiconductor pn diodes, vertical or lateral. See Glaxo Wellcome, 356 F.3d at 1355 ("the Supreme Court in Festo neither excuses an applicant from failing to claim 'readily known equivalents' at the time of application nor allows a patentee to rebut the Festo presumption by invoking its own failure to include a known equivalent in its original disclosure"). Accordingly, Oki fails to overcome the Festo presumption and may not proceed to assert infringement under the doctrine of equivalents.

AMD's motion for partial summary judgment of noninfringement of the Kurachi patents by its K8 processors is therefore GRANTED.

VII. Cross-Motions for Partial Summary Judgment of Infringement and Invalidity of the Sawamura Patent

1. Background

The Sawamura patent is entitled "Semiconductor Device." '855 patent at [54]. Oki is the assignee. Id. at [73]. The patent is directed to a semiconductor device that includes structural features, termed "dummy active regions," to ensure even abrasion of the surface during the required polishing steps. The invention also discloses and claims particular sizes

and shapes for the dummy active regions, and spacings between the dummy features and the active components on the semiconductor.

Fabrication of semiconductor devices composed of multiple layers requires planarization of each layer before addition of the next. As each layer, which contains active elements such as wire leads, transistors, diodes, MOSFETs, and the like, is completed, those elements are encased in an insulating oxide film. Before proceeding to fabricate another layer on top of this, the film is polished to create a smooth surface which is critical to the subsequent processing steps. It was observed, however, that the layout of active elements in a layer affected the polishing process because the hardness of the elements differed from that of the oxide present in areas lacking any elements. To counteract the uneven polishing (referred to as "dishing"), dummy regions composed of the same semiconductor material as the active elements are included in the device in areas lacking active elements. Thus, the average abrading speed across the entire device surface is evened out to provide a smooth, flat finish.

The dummy active regions must also be isolated from the active regions to prevent any electrical contact between these dummy and active areas. The patent discloses as the isolation region a trench filled with an oxide film formed by a high density plasma chemical vapor deposition ("HDP-CVD") method.

Despite the general knowledge of those skilled in the art regarding the need for dummy regions and isolation trenches, several shortcomings were not fully appreciated. The patentee disclosed that making rectangular or square dummy regions, limiting the short side of the dummy region to between 0.5 - 1.0 m, and/or spacing the dummy and actives regions apart by 0.5 - 10.0 m, yielded an improved device for the following reasons: the oxide film would form with a vertex and not a flat expense that is more difficult to polish, and the isolation region would be larger than the size of particulate impurities but narrow enough to avoid dishing.

Oki asserts claims 1, 6, and 7 against various processor families made by AMD under the theory of literal infringement or infringement by the doctrine of equivalents.

2. The Cross-Motions

Oki moves for partial summary judgment of infringement of claim 1 under the doctrine of equivalents, literal infringement of claim 6, and infringement of claim 7 under both theories. Oki alleges that AMD's expert witness does not disagree with Oki's expert's conclusion of infringement. In response, AMD contends that there is at least a genuine issue of material fact regarding the spacing between elements, and refers to its cross-motion for invalidity which highlights that an invalid patent cannot be infringed.

AMD cross-moves for invalidity of all three asserted claims of the Sawamura patent under 35 U.S.C. section 102(b). AMD's motion alleges that the invention was in public use or on sale more than one year prior to the filing date of the patent: the Pentium 233 MHz processor sold by Intel Corporation contains a trench region filled with an oxide, and dummy active regions, spaced and dimensioned according to the claims of Sawamura.

Oki contends that the Intel processor does not anticipate, and thereby invalidate, the claims because the isolation trench is filled using a plasma-enhanced CVD ("PE-CVD") process and not the HDP-CVD recited by the claims. Because anticipation must be predicated on identity, not just equivalency, of all elements, Oki asserts the motion must be denied.

3. Analysis

First, Oki does not contest AMD's assertion that the Intel processor anticipated claim 6. AMD's motion proffered Intel sales records establishing an on-sale date prior to the critical date, and third party testimony on and analysis of the sizing and spacing of dummy active regions in the Intel processor detailing the overlap of the claim scope with the processor. Accordingly, AMD's motion is granted as to claim 6. Anderson, 477 U.S. at 250 (summary judgment shall be granted "if there is no genuine issue as to any material fact and if the moving party is entitled to judgment as a matter of law").

Oki's only response to AMD's motion is that the Intel processor did not anticipate claims 1 and 7, both of which include the limitation "an isolation region formed on the semiconductor substrate includ[ing] a trench filled with a high density plasma chemical

vapor deposition layer." '855 patent at 5:31-33, 6:13, 22-23. The Court finds, as movant AMD points out, that Oki does not dispute any of the remaining limitations of claim 1. Furthermore, claim 7 only adds the above quoted limitation to independent claim 6, which, as noted, is conceded as being anticipated. The parties agree that the isolation region of the Intel processor was prepared by a plasma-enhanced CVD process, which in a literal sense, is not the same as HDP-CVD. The parties disagree, however, as to whether this literal difference matters with respect to the scope of the claim. Thus, the Court now construes the above claim limitation as a threshold step before determining whether the Intel prior art device anticipates or whether the accused products infringe the claims.

a. Construction of "a trench filled with a high density plasma chemical vapor deposition layer"

Claims 1 and 7 are device claims directed to a semiconductor product comprising an active region, a dummy active region, and an isolation region as structural features. The claims further describe the isolation region as "including a trench filled with a high density plasma chemical vapor deposition layer." Id. at 5:31-33, 6:22-23. The parties differ over the meaning of this phrase. Oki contends that the literal phrase "high density plasma chemical vapor deposition" ("HDP-CVD") is an explicit structural limitation that must be given meaning, and to allow the claim scope to include oxides made by other processes would be to read this limitation out of the claims. AMD asserts instead that HDP-CVD is just the preferred method, and the claims should not be limited to a preferred method unless there is a clear intent to limit the claim scope.

The plain meaning of the claim reveals that the semiconductor device product is ultimately recited in terms of the structure of the product of a process for filling a trench in an isolation region. The claim requires that the trench is "filled with a high density plasma chemical vapor deposition layer." In one view, this is readily understood to mean the oxide layer product filling the trench is produced by a high density plasma chemical vapor deposition process; that is to say, the limitation is a product-by-process limitation. Oki contends, however, that this phrase should be read as a structural limitation. Another way to

read the limitation, emphasizing the structural aspect of the layer, is: a trench filled with a layer having the structure of an oxide produced by high density plasma chemical vapor deposition. But this analysis reaches the same conclusion as that which follows from a product-by-process limitation: the structure produced by the process is the subject of the claim. Although a gerund phrase does not introduce the deposition process, such as, "filling the trench by an HDP-CVD process," as in the typical format of process claims, one of skill in the art is left with the inescapable conclusion that the claim is drawn to the product of the deposition process.

"Regardless of how broadly or narrowly one construes a product-by-process claim, it is clear that such claims are always to a product, not a process." Smithkline Beecham Corp. v. Apotex Corp., 439 F.3d 1312, 1317 (Fed. Cir. 2006). The specification refers to the trench being filled with an embedded oxide film. See '855 patent at 2:18-24. The process for forming the oxide film is exemplified as being an HDP-CVD process, but under the analytical principals reaffirmed in Smithkline, the claim term is compared with the prior art on the basis of what the product is, and not with reference to the particular process for forming the embedded oxide film. See 439 F.3d at 1317-18.

The only qualification the patentee placed on the structure of the oxide film was that it be a "good quality oxide film." '855 patent at 2:22-24. Expert testimony proffered by AMD informs that a film is of "good quality" when the film does not have gaps or voids. AMD's Mot. Partial Summ. J., Exh. F (Neikirk Report) at ¶ 95. Oki's technical expert implies the same in his statement that "[a]n important aspect of advanced semiconductor device isolation is the filling of etched shallow trenches without the occurrence of voids in the deposited film." Kirsch Decl., Exh. B (Expert Report of Dr. Fair) at ¶ 211. No other advantageous qualities or distinguishing properties were disclosed by the patentee. Oki's expert confirmed this finding, stating that nothing in the claims, specification, or file history "would specially limit an HDPCVD layer as a trench fill layer compared to other CVD layers." Id. at ¶ 213.

The Court construes the limitation "a trench filled with a high density plasma chemical vapor deposition layer" to mean an oxide film layer having the structure of that

which is produced by high density plasma chemical vapor deposition, but not limited to formation by that process, such that the film completely fills the trench without gaps or voids.

b. Application of the construed terms to the motions

The isolation region trench on the Intel processor is filled with an oxide film by a multi-step chemical vapor deposition process. The three steps in the Intel process include (1) oxide deposition by plasma-enhanced chemical vapor deposition, (2) argon plasma sputter etch, and (3) another oxide deposition by PE-CVD. See Mot., Exh. O (Intel Process Documents) at 850AMD000018-22. In comparison, the HDP-CVD process recited in the claims operates by three principal mechanisms: "[1] ion-assisted plasma deposition, [2] argon sputtering, and [3] re-deposition of the sputtered material." Kirsch Decl., Exh. B (Expert Report of Dr. Fair) at ¶ 212. Thus, the oxide film formation occurs through the same mechanism, albeit in three steps in the Intel process and in one step in the HDP-CVD process. Although specific differences exist between the processes, such as the density of the plasma source and the bias applied to the substrate, this does not alter the conclusion that the oxide films produced by Intel disclosed to those skilled in the art each and every element of the claim. The product oxide films are indistinguishable from the viewpoint of the product structure as claimed. See Motorola, 121 F.3d at 1473. Once a product is fully disclosed in the art, future claims to that same product are precluded, even if that product is claimed as made by a new process. Smithkline, 439 F.3d at 1315.

Accordingly, AMD's motion for partial summary judgment of invalidity must be GRANTED because all the elements of claims 1, 6, and 7 are found in an Intel processor on sale more than one year prior to the filing date of the Sawamura patent, and Oki's motion for partial summary judgment of infringement must be DENIED.

IT IS SO ORDERED.

Dated: November 13, 2006

CHARLES R. BREYER
UNITED STATES DISTRICT JUDGE